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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/905,542	07/13/2001	Masaaki Hiroki	SEL 269	3940

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EXAMINER	
EISEN, ALEXANDER	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/905,542	HIROKI ET AL.	
	Examiner	Art Unit	
	Alexander Eisen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,16-27 and 39-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,16-27 and 39-65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 17-24 and 39-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirakata in view of Mori (both are references of record) and further in view of Soneda et al., ("Soneda"), JP 61-069283.

With respect to claims 1, 20 and 21, Hirakata discloses a semiconductor device (FIGS. 1A-B) and associated with it method of driving the same, the device comprising a plurality of switching elements SW1-SW4; a plurality of pixel electrodes LC; an opposing electrode (col. 3, ll. 32-40), wherein a display signal is input to the plurality of pixel electrodes through the plurality of switching elements; all of the display signals input to the plurality of pixel electrodes have the same polarity within each frame period, with the electric potential of the opposing electrode as a reference; the frame rate conversion portion operates in synchronous with the display signals; and among two arbitrary, adjacent frame periods, the display signal input to the plurality of pixels in the latter frame period to appear has an electric potential which is an inversion of the display signal input to the plurality of pixels in the former frame period, with the electric potential of the opposing electrode as a reference (see FIG. 11A; col. 1, ll. 19-35).

Hirakata does not disclose that the semiconductor device includes a frame rate conversion portion.

Mori teaches a frame rate conversion control system (FIGS. 5-7; col. 2, ll. 10-53) for LCD.

It would have been obvious to one of ordinary skill in the art at the time when the invention was made to use frame rate control system taught by Mori in the semiconductor display device of Hirakata, because it would reduce a flicker while preventing a sticking (col. 2, ll. 54-63).

None of the above teach that a same image is displayed in a pixel portion in the two arbitrary, adjacent frame periods.

Soneda teaches that when an image to be displayed represents still image, same image is displayed in the two arbitrary, adjacent frame periods, and therefore it would have been obvious to one of ordinary skill in the art at the time when the invention was made that the display of Mori-Hirakata will display a same image in the two arbitrary, adjacent frame periods, when the image to be displayed is a still image.

As to claims 2 and 22, Hirakata also teaches a method of driving whereby within each frame period display signals having mutually inverse polarities, with the electric potential of the opposing electrode as a reference, are input to source signal lines which are adjacent to the plurality of source signal lines; and the display signals input to each of the plurality of source signal line always have the same polarity, with the electric potential of the opposing electrode as a reference; the frame rate conversion portion operates in synchronous with the display signals; and among two arbitrary, adjacent frame periods, the display signal input to the plurality of pixels in the latter frame period to appear has an electric potential which is an inversion of the

display signal input to the plurality of pixels in the former frame period, with the electric potential of the opposing electrode as a reference (i.e. data line inversion as in FIG. 11B).

As to claims 3 and 23, Hirakata also teaches a method of driving whereby within each frame period the display signals input to all of the plurality of source signal lines always have the same polarity, with the electric potential of the opposing electrode as a reference; the polarities of the display signals input to the plurality of source signal lines are mutually inverted in adjacent line periods, with the electric potential of the opposing electrode as a reference; the frame rate conversion portion operates in synchronous with the display signals; and among two arbitrary, adjacent frame periods, the display signal input to the plurality of pixels in the latter frame period to appear has an electric potential which is an inversion of the display signal input to the plurality of pixels in the former frame period, with the electric potential of the opposing electrode as a reference (i.e. row inversion as in FIG. 11C).

As to claims 4 and 24, Hirakata further discloses a method wherein within each frame period display signals having mutually inverse polarities, with the electric potential of the opposing electrode as a reference, are input to source signal lines adjacent to the plurality of source signal lines; the polarities of the display signals input to the plurality of source signal lines are mutually inverted in adjacent line periods, with the electric potential of the opposing electrode as a reference; the frame rate conversion portion operates in synchronous with the display signals; and among two arbitrary, adjacent frame periods, the display signal input to the plurality of pixels in the latter frame period to appear has an electric potential which is an inversion of the display signal input to the plurality of pixels in the former frame period, with the electric potential of the opposing electrode as a reference (dot inversion scheme as in FIG. 11D).

As to claims 17-19 and 39-65, the use of semiconductor display devices in computers, cameras and DVD players is well known in the art, and therefore it would be obvious to one of ordinary skill in the art that the display device of Hirakata, as modified by Mori, would not be excluded from use in such electronic devices.

3. Claims 16 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirakata in view of Mori, as applied to claim 1, and further in view of Koyama, US 5,942,856.

Hirakata and Mori do not teach that the switching element is a transistor formed using single crystal silicon, a thin film transistor formed using polycrystalline silicon or a thin film transistor formed using amorphous silicon.

Koyama teaches that the switching elements for pixels can be made of polycrystalline silicon or amorphous silicon (col. 1, ll. 12-18; col. 6, ll. 37-41).

It would have been obvious to one of ordinary skill in the art at the time when the invention was made that the switching elements SW in Hirakata can be made of any known to artisans at that time semiconductor materials, as taught by Koyama, without bringing about any unexpected result, whereby a choice would be at discretion of a designer.

Response to Arguments

4. Applicant's arguments with respect to claims 1-4, 16-27 and 39-65 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Eisen whose telephone number is (571) 272-7687. The examiner can normally be reached on M-F (9:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

2 September 2005

Alexander Eisen
Primary Examiner
Art Unit 2674